µA741 General-Purpose Operational Amplifiers

1 Features

- Short-Circuit Protection
- Offset-Voltage Null Capability
- Large Common-Mode and Differential Voltage Ranges
- No Frequency Compensation Required
- No Latch-Up

2 Applications

- DVD Recorders and Players
- Pro Audio Mixers

3 Description

The µA741 device is a general-purpose operational amplifier featuring offset-voltage null capability.

The high common-mode input voltage range and the absence of latch-up make the amplifier ideal for voltage-follower applications. The device is short-circuit protected and the internal frequency compensation ensures stability without external components. A low value potentiometer may be connected between the offset null inputs to null out the offset voltage as shown in Figure 11.

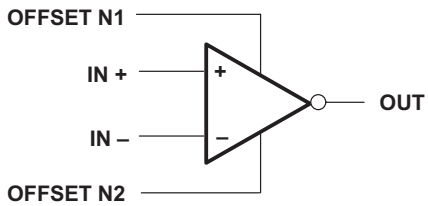
The µA741C device is characterized for operation from 0°C to 70°C. The µA741M device (obsolete) is characterized for operation over the full military temperature range of –55°C to 125°C.

Device Information(1)

PART NUMBER	PACKAGE (PIN)	BODY SIZE (NOM)
µA741x	SOIC (8)	4.90 mm × 3.91 mm
	PDIP (8)	9.81 mm × 6.35 mm
	SO (8)	6.20 mm × 5.30 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Simplified Schematic



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5 Revision History

Changes from Revision D (February 2014) to Revision E — **Page**

- Added *Applications*, *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Moved *Typical Characteristics* into *Specifications* section. ... 7

Changes from Revision C (January 2014) to Revision D — **Page**

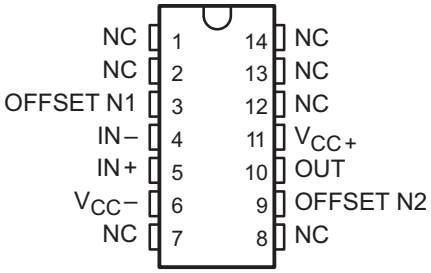
- Fixed *Typical Characteristics* graphs to remove extra lines. ... 7

Changes from Revision B (September 2000) to Revision C — **Page**

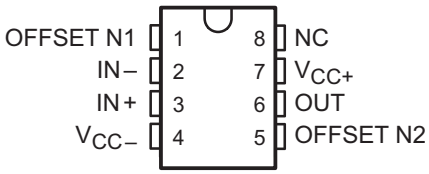
- Updated document to new TI data sheet format - no specification changes. ... 1
- Deleted *Ordering Information* table. ... 1

6 Pin Configurations and Functions

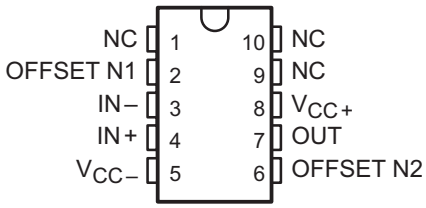
µA741M . . . J PACKAGE
(TOP VIEW)



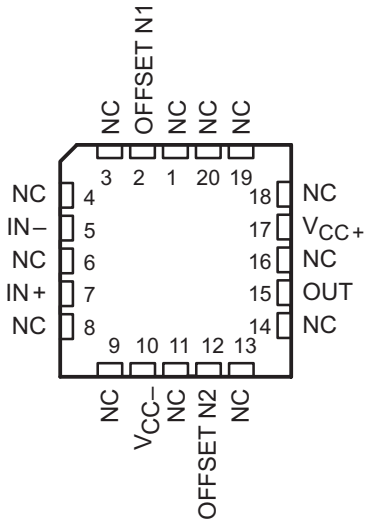
µA741M . . . JG PACKAGE
µA741C, µA741I . . . D, P, OR PW PACKAGE
(TOP VIEW)



µA741M . . . U PACKAGE
(TOP VIEW)



µA741M . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

Pin Functions

NAME	PIN				TYPE	DESCRIPTION
	J	JG, D, P, or PW	U	FK		
IN+	5	3	4	7	I	Noninverting input
IN–	4	2	3	5	I	Inverting input
NC	1, 2, 8, 12, 13, 14	8	1, 9, 10	1,3,4,6,8,9,11,13,14,16,18,19,20	—	Do not connect
OFFSET N1	3	1	2	2	I	External input offset voltage adjustment
OFFSET N2	9	5	6	12	I	External input offset voltage adjustment
OUT	10	6	7	15	O	Output
V_{CC}+	11	7	8	17	—	Positive supply
V_{CC}–	6	4	5	10	—	Negative supply

7 Specifications

7.1 Absolute Maximum Ratings

over virtual junction temperature range (unless otherwise noted)(1)

			μA741C		μA741M		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage(2)		–18	18	–22	22	C
V_{ID}	Differential input voltage(3)		–15	15	–30	30	V
V_I	Input voltage, any input(2)(4)		–15	15	–15	15	V
	Voltage between offset null (either OFFSET N1 or OFFSET N2) and $V_{CC–}$		–15	15	–0.5	0.5	V
	Duration of output short circuit(5)		Unlimited				
	Continuous total power dissipation		See Table 1				
T_A	Operating free-air temperature range		0	70	–55	125	°C
	Case temperature for 60 seconds	FK package	N/A	N/A		260	°C
	Lead temperature 1.6 mm (1/16 inch) from case for 60 seconds	J, JG, or U package	N/A	N/A		300	°C
	Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	D, P, or PS package		260	N/A	N/A	°C
T_{stg}	Storage temperature range		–65	150	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and $V_{CC–}$.
(3) Differential voltages are at IN+ with respect to IN –.
(4) The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
(5) The output may be shorted to ground or either power supply. For the μA741M only, the unlimited duration of the short circuit applies at (or below) 125°C case temperature or 75°C free-air temperature.

7.2 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC+}	Supply voltage		5	15	V
$V_{CC–}$			–5	–15	
T_A	Operating free-air temperature	μA741C	0	70	°C
		μA741M	–55	125	

Table 1. Dissipation Ratings Table

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	TA = 70°C POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	500 mW	5.8 mW/°C	64°C	464 mW	377 mW	N/A
FK	500 mW	11.0 mW/°C	105°C	500 mW	500 mW	275 mW
J	500 mW	11.0 mW/°C	105°C	500 mW	500 mW	275 mW
JG	500 mW	8.4 mW/°C	90°C	500 mW	500 mW	210 mW
P	500 mW	N/A	N/A	500 mW	500 mW	N/A
PS	525 mW	4.2 mW/°C	25°C	336 mW	N/A	N/A
U	500 mW	5.4 mW/°C	57°C	432 mW	351 mW	135 mW

7.3 Electrical Characteristics µA741C, µA741M

at specified virtual junction temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A (1)	µA741C			µA741M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0	25°C		1	6		1	5	mV
			Full range			7.5		±15	6	
$\Delta V_{IO(adj)}$	Offset voltage adjust range	V_O = 0	25°C		±15			20	200	mV
I_{IO}	Input offset current	V_O = 0	25°C		20	200			500	nA
			Full range			300			500	
I_{IB}	Input bias current	V_O = 0	25°C		80	500		80	500	nA
			Full range			800			1500	
V_{ICR}	Common-mode input voltage range		25°C	±12	±13		±12	±13		V
			Full range	±12			±12			
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ	25°C	±12	±14		±12	±14		V
		R_L ≥ 10 kΩ	Full range	±12			±12			
		R_L = 2 kΩ	25°C	±10			±10	±13		
		R_L ≥ 2kΩ	Full range	±10			±10			
A_{VD}	Large-signal differential voltage amplification	R_L ≥ 2kΩ	25°C	20	200		50	200		V/mV
		V_O = ±10 V	Full range	15			25			
r_i	Input resistance		25°C	0.3	2		0.3	2		MΩ
r_o	Output resistance	V_O = 0, See (2)	25°C		75			75		Ω
C_i	Input capacitance		25°C		1.4			1.4		pF
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICRmin}	25°C	70	90		70	90		dB
			Full range	70			70			
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	V_{CC} = ±9 V to ±15 V	25°C		30	150		30	150	µV/V
			Full range			150			150	
I_{OS}	Short-circuit output current		25°C		±25	±40		±25	±40	mA
I_{CC}	Supply current	V_O = 0, No load	25°C		1.7	2.8		1.7	2.8	mA
			Full range			3.3			3.3	
P_D	Total power dissipation	V_O = 0, No load	25°C		50	85		50	85	mW
			Full range			100			100	

(1) All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for the µA741C is 0°C to 70°C and the µA741M is –55°C to 125°C.
(2) This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

7.4 Electrical Characteristics µA741Y

at specified virtual junction temperature, $V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	µA741Y			UNIT
			MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0		1	5	mV
$\Delta V_{IO(adj)}$	Offset voltage adjust range	V_O = 0		±15		mV
I_{IO}	Input offset current	V_O = 0		20	200	nA
I_{IB}	Input bias current	V_O = 0		80	500	nA
V_{ICR}	Common-mode input voltage range		±12	±13		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ	±12	±14		V
		R_L = 2 kΩ	±10	±13		
A_{VD}	Large-signal differential voltage amplification	R_L ≥ 2kΩ	20	200		V/mV
r_i	Input resistance		0.3	2		MΩ
r_o	Output resistance	V_O = 0, See(1)		75		Ω
C_i	Input capacitance			1.4		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICRmin}$	70	90		dB
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	V_{CC} = ±9 V to ±15 V		30	150	µV/V
I_{OS}	Short-circuit output current			±25	±40	mA
I_{CC}	Supply current	V_O = 0, No load		1.7	2.8	mA
P_D	Total power dissipation	V_O = 0, No load		50	85	mW

(1) This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

7.5 Switching Characteristics µA741C, µA741M

over operating free-air temperature range, $V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	µA741C			µA741M			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise time	V_I = 20 mV, R_L = 2 kΩ, C_L = 100 pF, See Figure 1		0.3			0.3		µs
	Overshoot factor			5%			5%		—
SR	Slew rate at unity gain	V_I = 10 V, R_L = 2 kΩ, C_L = 100 pF, See Figure 1		0.5			0.5		V/µs

7.6 Switching Characteristics µA741Y

over operating free-air temperature range, $V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	µA741Y			UNIT
			MIN	TYP	MAX	
t_r	Rise time	V_I = 20 mV, R_L = 2 kΩ, C_L = 100 pF, See Figure 1		0.3		µs
	Overshoot factor			5%		—
SR	Slew rate at unity gain	V_I = 10 V, R_L = 2 kΩ, C_L = 100 pF, See Figure 1		0.5		V/µs

7.7 Typical Characteristics

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

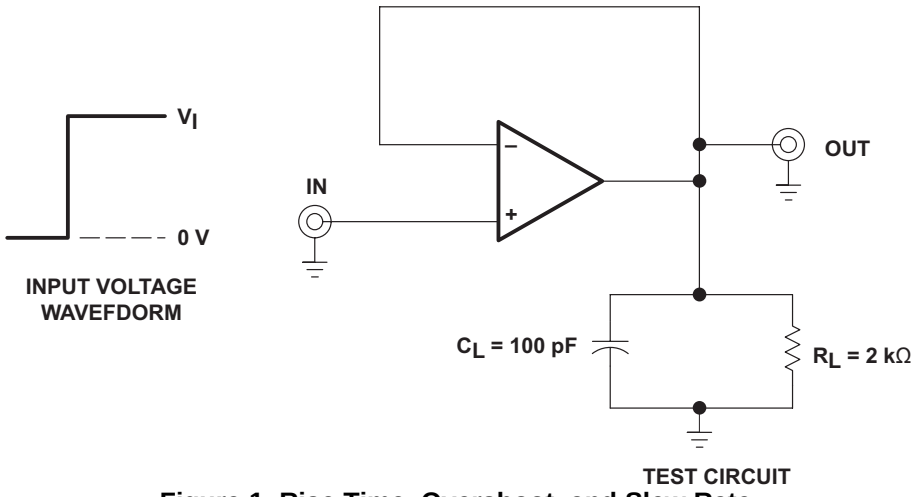


Figure 1. Rise Time, Overshoot, and Slew Rate

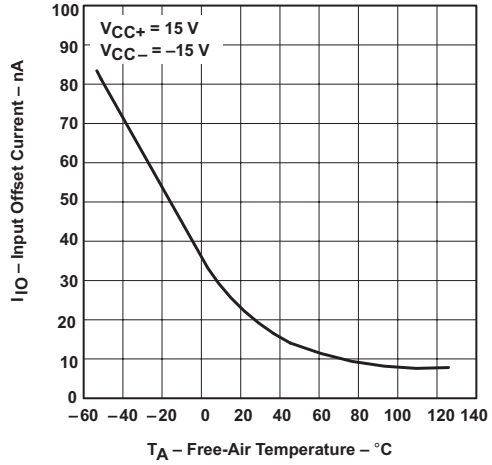


Figure 2. Input Offset Current vs Free-Air Temperature

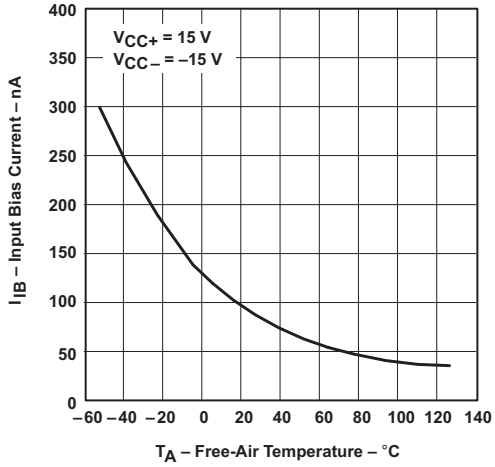


Figure 3. Input Bias Current vs Free-Air Temperature

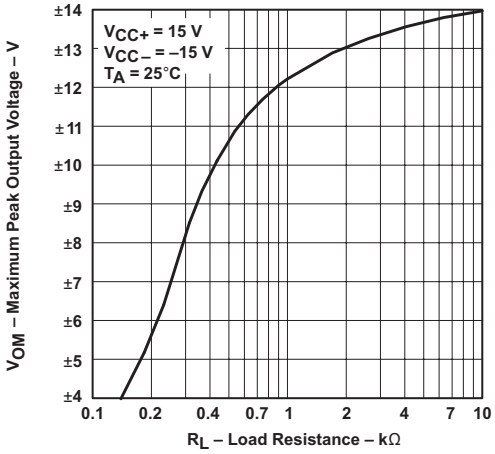


Figure 4. Maximum Output Voltage vs Load Resistance

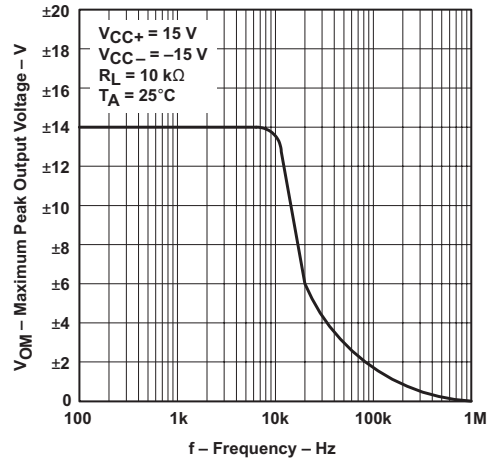


Figure 5. Maximum Peak Output Voltage vs Frequency

Typical Characteristics (continued)

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

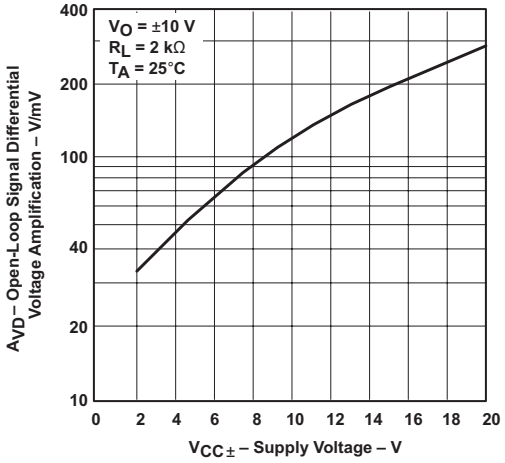


Figure 6. Open-Loop Signal Differential Voltage Amplification vs Supply Voltage

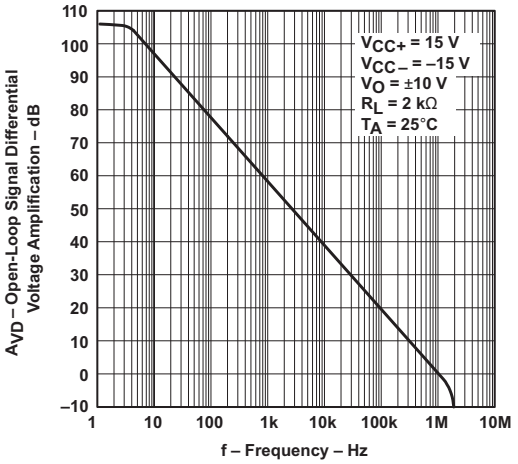


Figure 7. Open-Loop Large-Signal Differential Voltage Amplification vs Frequency

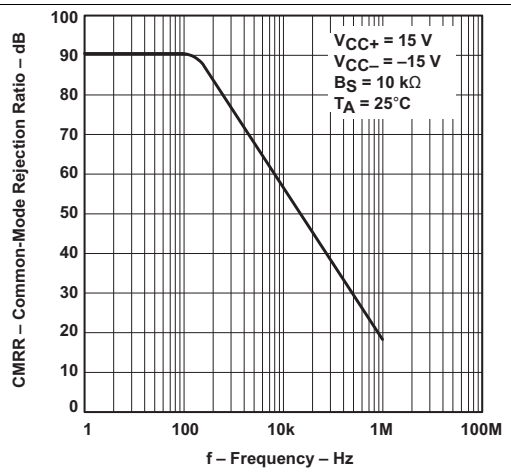


Figure 8. Common-Mode Rejection Ratio vs Frequency

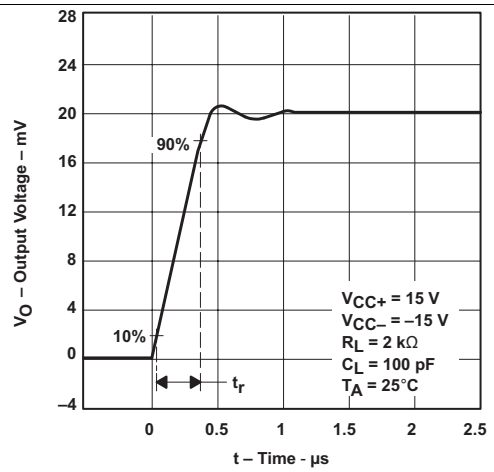


Figure 9. Output Voltage vs Elapsed Time

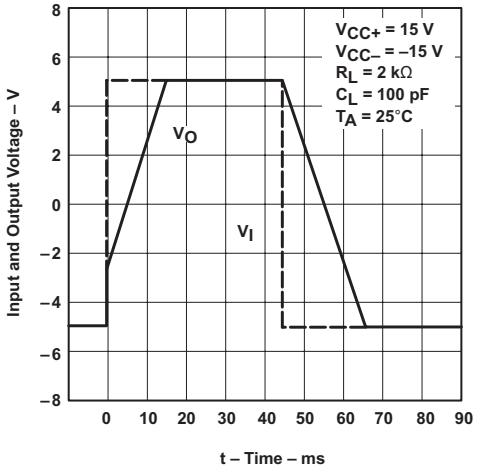


Figure 10. Voltage-Follower Large-Signal Pulse Response

8 Detailed Description

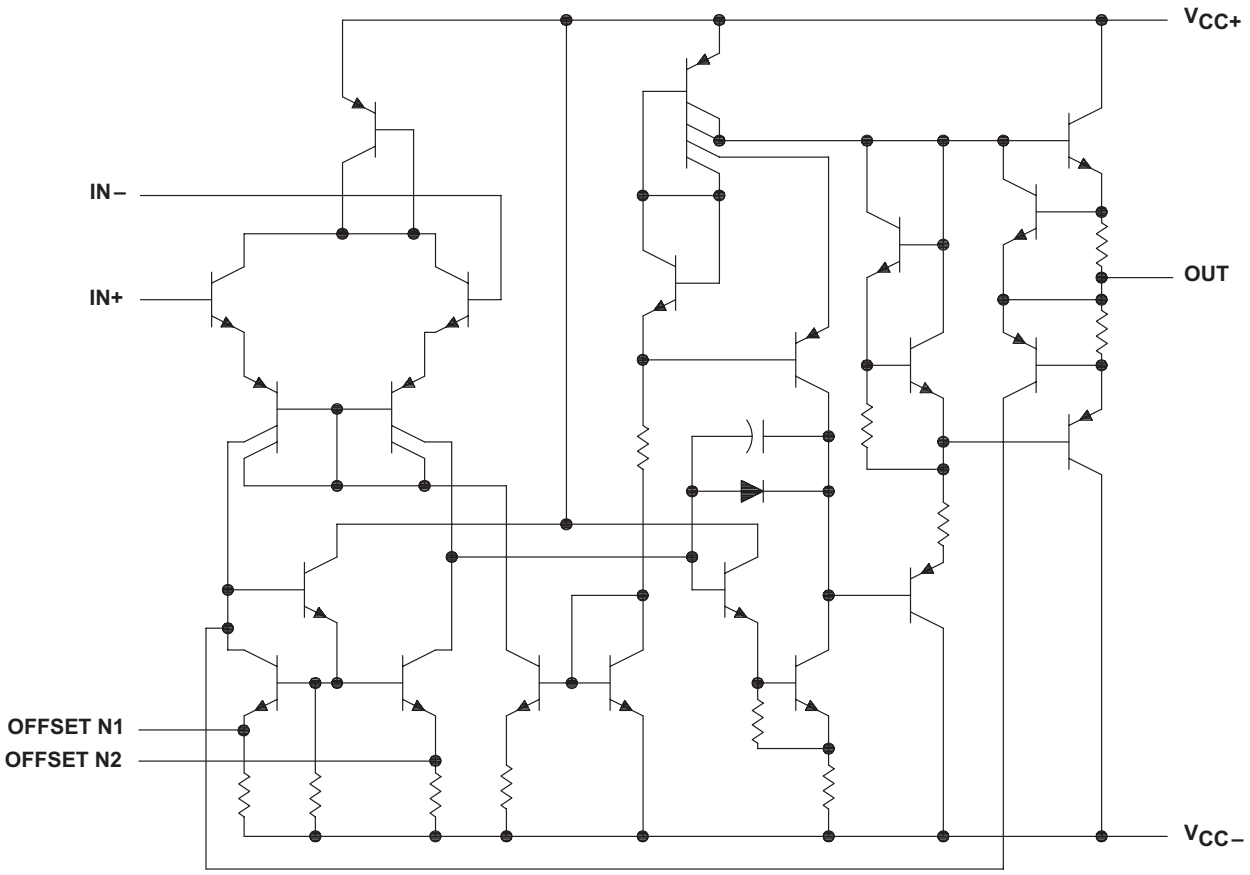
8.1 Overview

The µA741 device is a general-purpose operational amplifier featuring offset-voltage null capability.

The high common-mode input voltage range and the absence of latch-up make the amplifier ideal for voltage-follower applications. The device is short-circuit protected and the internal frequency compensation ensures stability without external components. A low value potentiometer may be connected between the offset null inputs to null out the offset voltage as shown in Figure 11.

The µA741C device is characterized for operation from 0°C to 70°C. The µA741M device (obsolete) is characterized for operation over the full military temperature range of –55°C to 125°C.

8.2 Functional Block Diagram



Component Count	
Transistors	22
Resistors	11
Diode	1
Capacitor	1

8.3 Feature Description

8.3.1 Offset-Voltage Null Capability

The input offset voltage of operational amplifiers (op amps) arises from unavoidable mismatches in the differential input stage of the op-amp circuit caused by mismatched transistor pairs, collector currents, current-gain betas (β), collector or emitter resistors, etc. The input offset pins allow the designer to adjust for these mismatches by external circuitry. See the *Application and Implementation* section for more details on design techniques.

8.3.2 Slew Rate

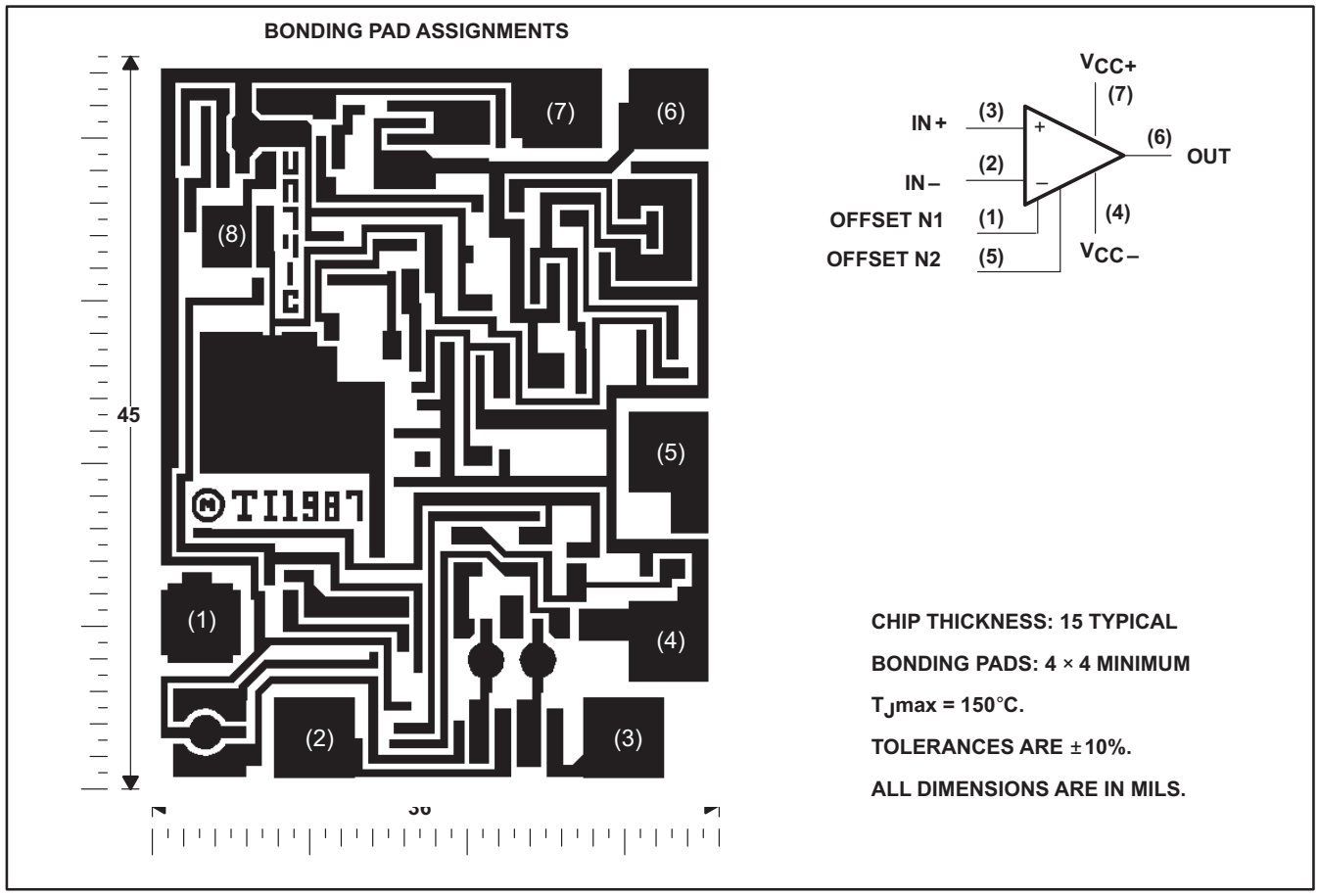
The slew rate is the rate at which an operational amplifier can change its output when there is a change on the input. The µA741 has a 0.5-V/µs slew rate. Parameters that vary significantly with operating voltages or temperature are shown in the *Typical Characteristics* graphs.

8.4 Device Functional Modes

The µA741 is powered on when the supply is connected. It can be operated as a single supply operational amplifier or dual supply amplifier depending on the application.

8.5 µA741Y Chip Information

This chip, when properly assembled, displays characteristics similar to the µA741C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.



9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The input offset voltage of operational amplifiers (op amps) arises from unavoidable mismatches in the differential input stage of the op-amp circuit caused by mismatched transistor pairs, collector currents, current-gain betas (β), collector or emitter resistors, etc. The input offset pins allow the designer to adjust for these mismatches by external circuitry. These input mismatches can be adjusted by putting resistors or a potentiometer between the inputs as shown in Figure 13. A potentiometer can be used to fine tune the circuit during testing or for applications which require precision offset control. More information about designing using the input-offset pins, see the application note *Nulling Input Offset Voltage of Operational Amplifiers*, SLOA045.

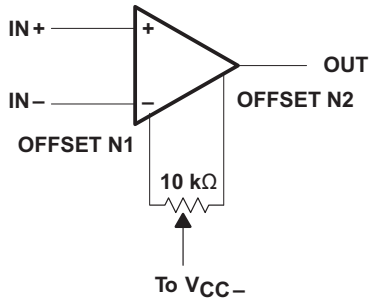


Figure 11. Input Offset Voltage Null Circuit

9.2 Typical Application

The voltage follower configuration of the operational amplifier is used for applications where a weak signal is used to drive a relatively high current load. This circuit is also called a buffer amplifier or unity gain amplifier. The inputs of an operational amplifier have a very high resistance which puts a negligible current load on the voltage source. The output resistance of the operational amplifier is almost negligible, so it can provide as much current as necessary to the output load.

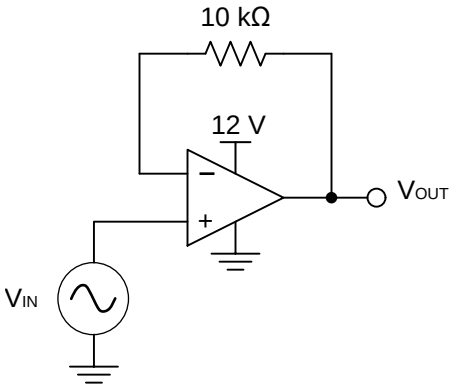


Figure 12. Voltage Follower Schematic

9.2.1 Design Requirements

- Output range of 2 V to 11.5 V
- Input range of 2 V to 11.5 V

Typical Application (continued)

- Resistive feedback to negative input

9.2.2 Detailed Design Procedure

9.2.2.1 Output Voltage Swing

The output voltage of an operational amplifier is limited by its internal circuitry to some level below the supply rails. For this amplifier, the output voltage swing is within ±12 V, which accommodates the input and output voltage requirements.

9.2.2.2 Supply and Input Voltage

For correct operation of the amplifier, neither input must be higher than the recommended positive supply rail voltage or lower than the recommended negative supply rail voltage. The chosen amplifier must be able to operate at the supply voltage that accommodates the inputs. Because the input for this application goes up to 11.5 V, the supply voltage must be 12 V. Using a negative voltage on the lower rail rather than ground allows the amplifier to maintain linearity for inputs below 2 V.

9.2.3 Application Curves for Output Characteristics

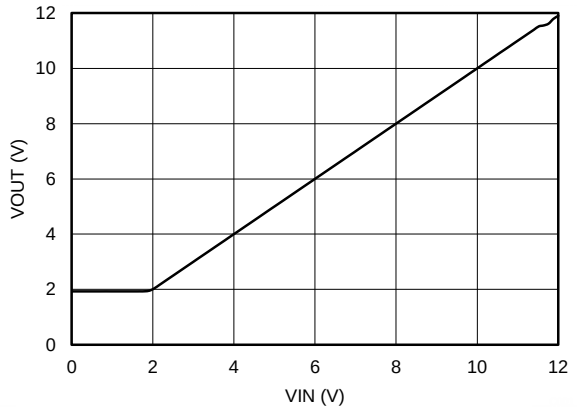


Figure 13. Output Voltage vs Input Voltage

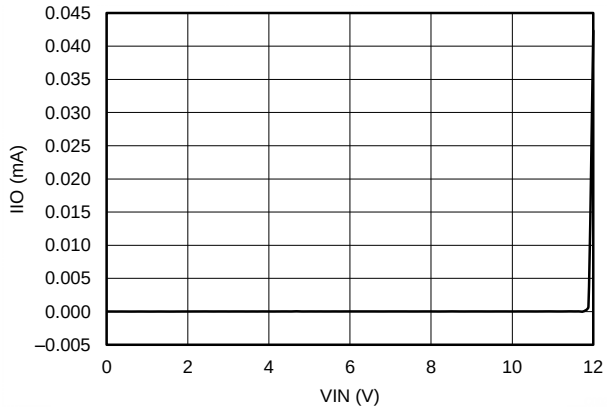


Figure 14. Current Drawn Input of Voltage Follower (I_{IO}) vs Input Voltage

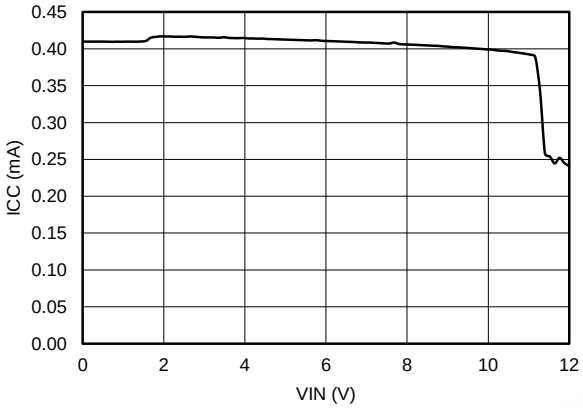


Figure 15. Current Drawn from Supply (I_{CC}) vs Input Voltage

10 Power Supply Recommendations

The µA741 is specified for operation from ±5 to ±15 V; many specifications apply from 0°C to 70°C. The *Typical Characteristics* section presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than ±18 V can permanently damage the device (see the *Absolute Maximum Ratings*).

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, refer to the *Layout Guidelines*.

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, refer to *Circuit Board Layout Techniques*, SLOA089.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in *Layout Example*.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

11.2 Layout Example

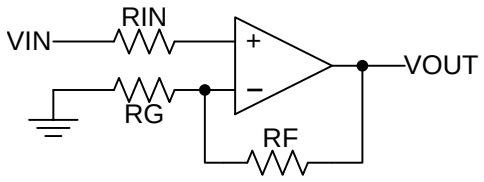


Figure 16. Operational Amplifier Schematic for Noninverting Configuration

Layout Example (continued)

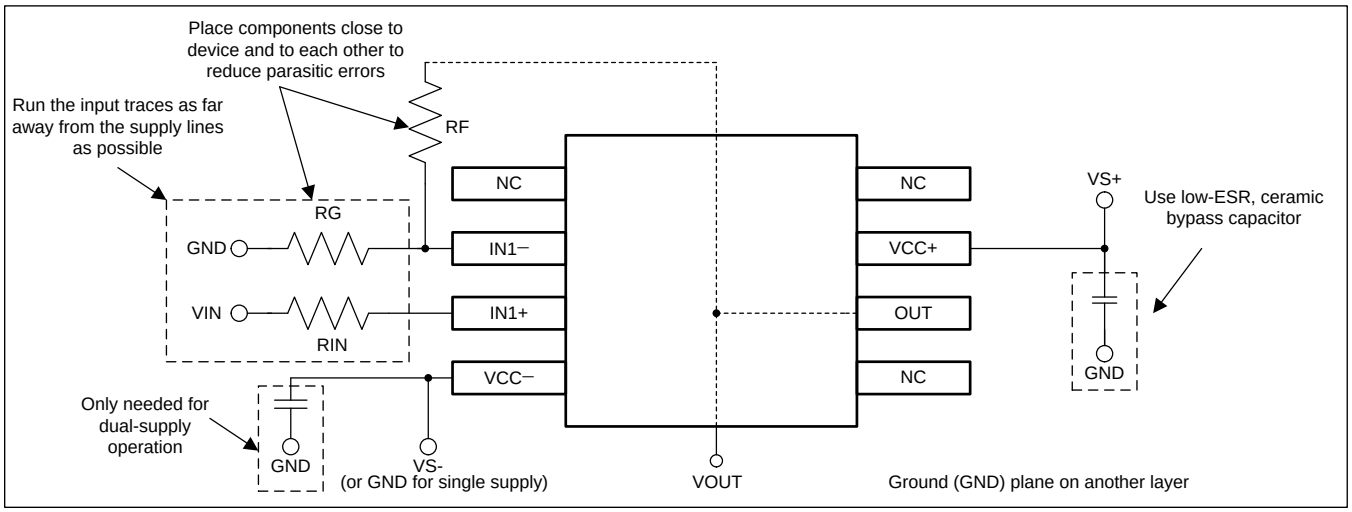


Figure 17. Operational Amplifier Board Layout for Noninverting Configuration

12 Device and Documentation Support

12.1 Trademarks

All trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UA741CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UA741C	Samples
UA741CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UA741C	Samples
UA741CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UA741C	Samples
UA741CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UA741C	Samples
UA741CP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	UA741CP	Samples
UA741CPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	UA741CP	Samples
UA741CPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	U741	Samples
UA741CPSRE4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	U741	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

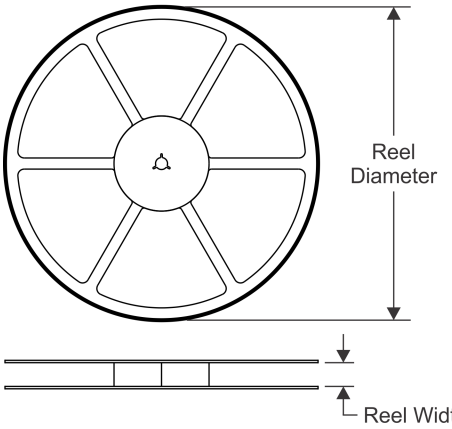
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

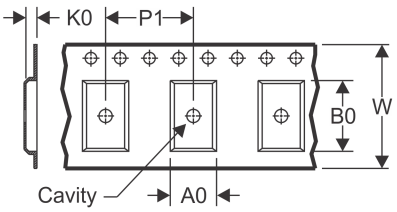
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

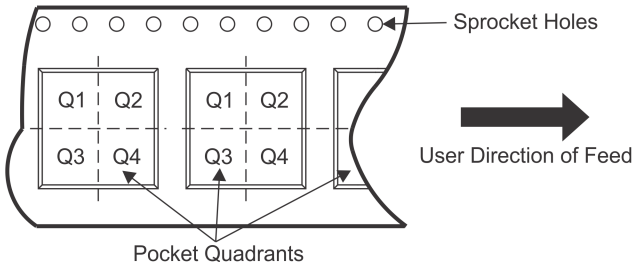


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

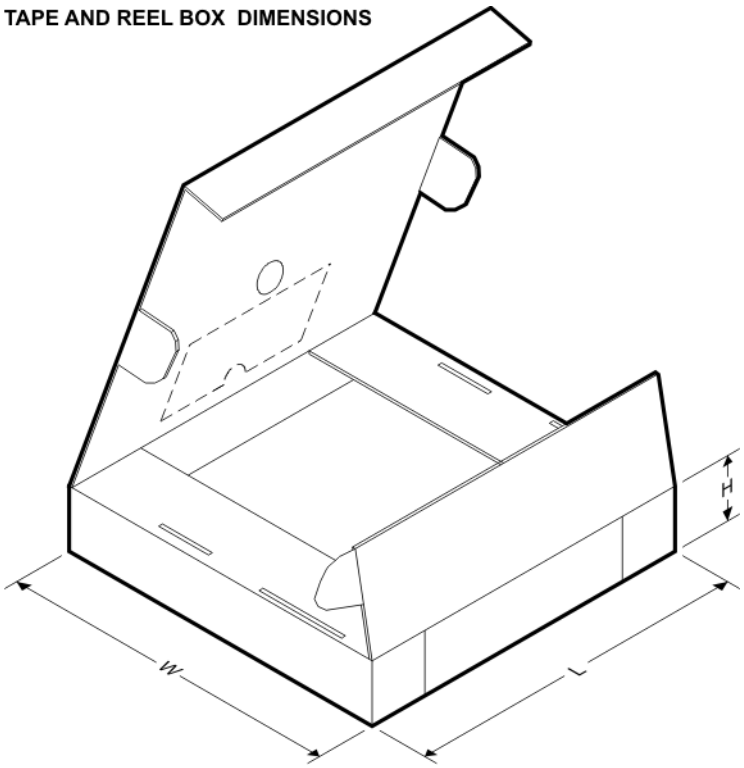
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UA741CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UA741CPSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1

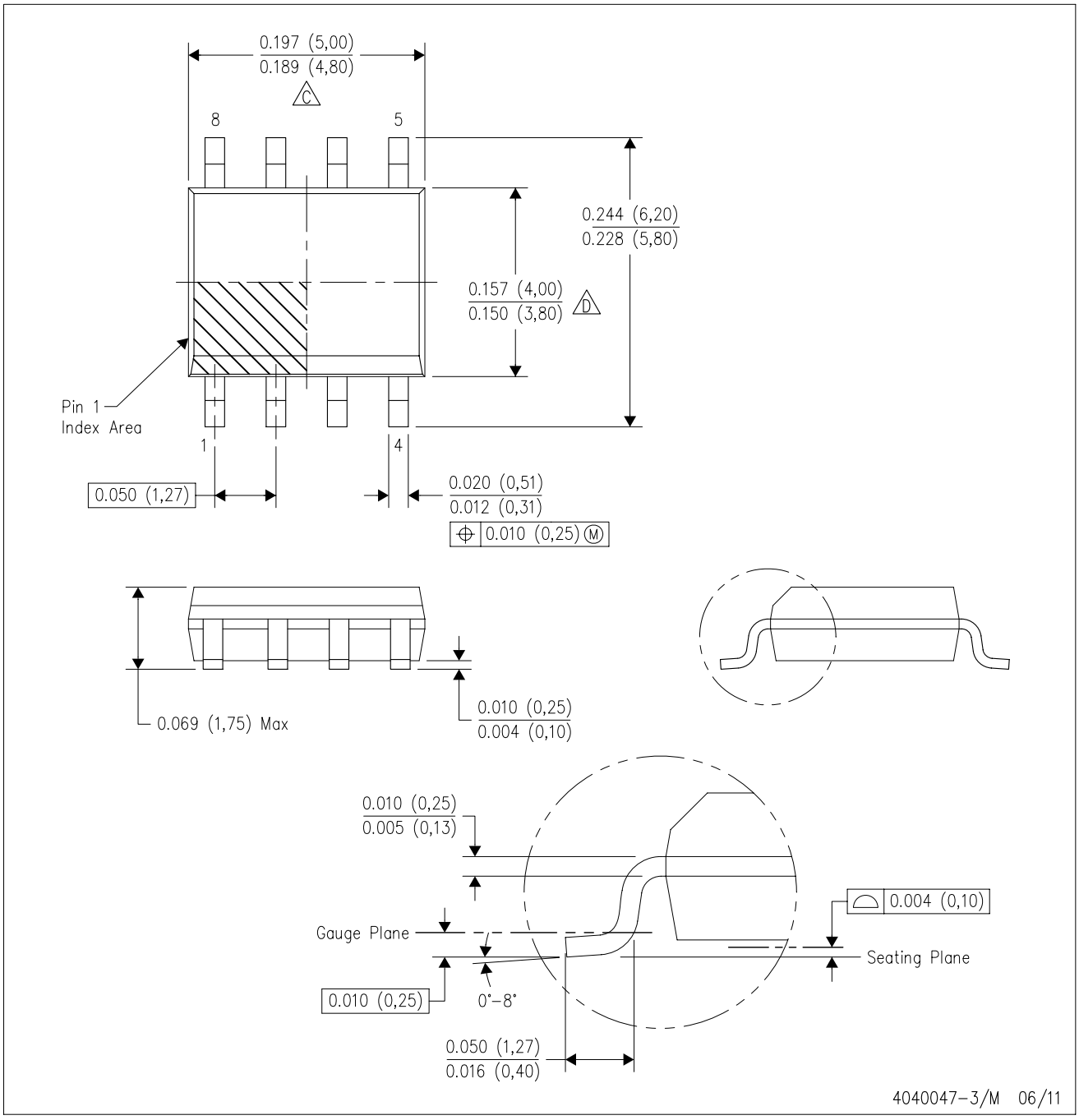
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

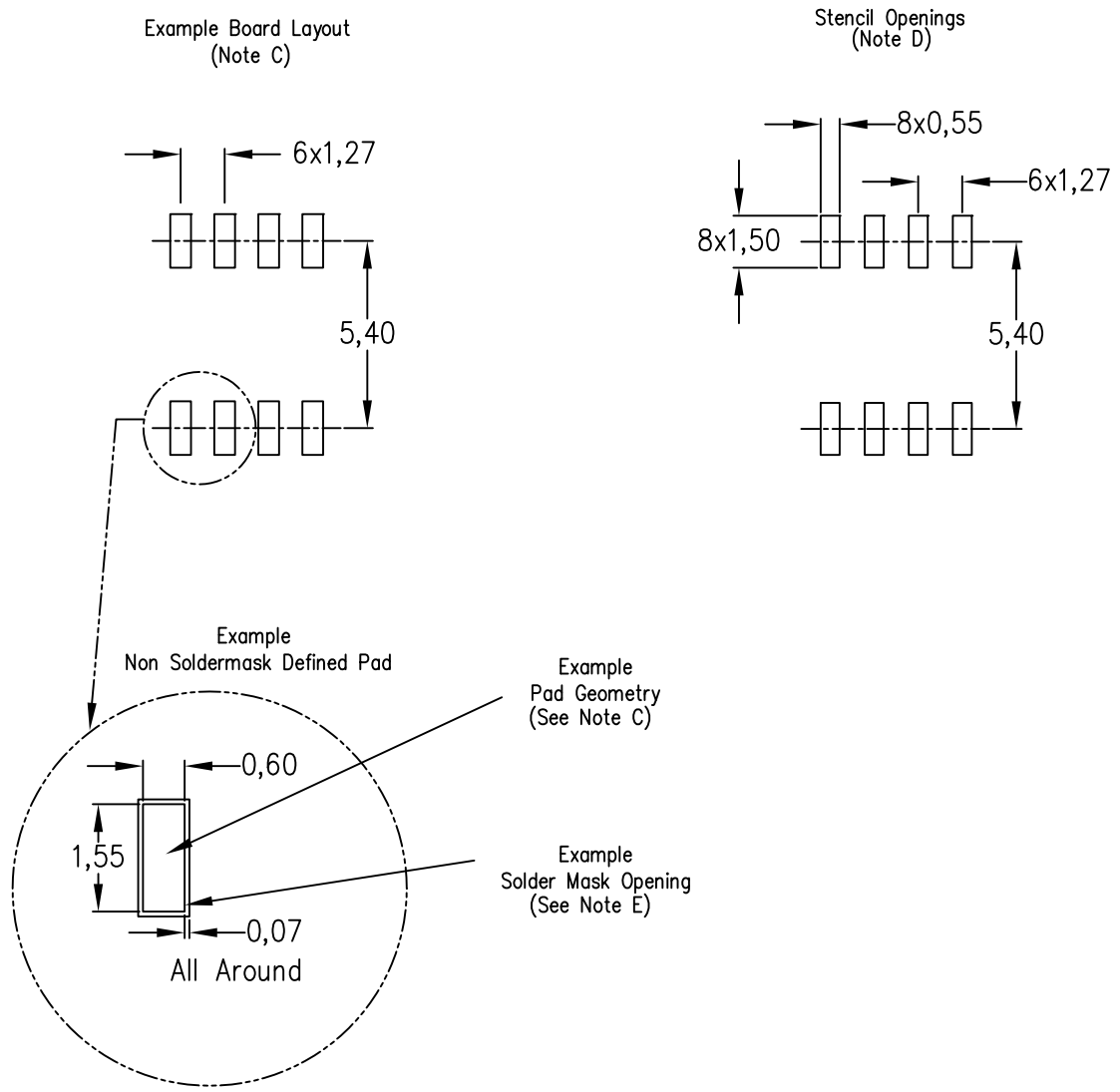
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UA741CDR	SOIC	D	8	2500	340.5	338.1	20.6
UA741CPSR	SO	PS	8	2000	367.0	367.0	38.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

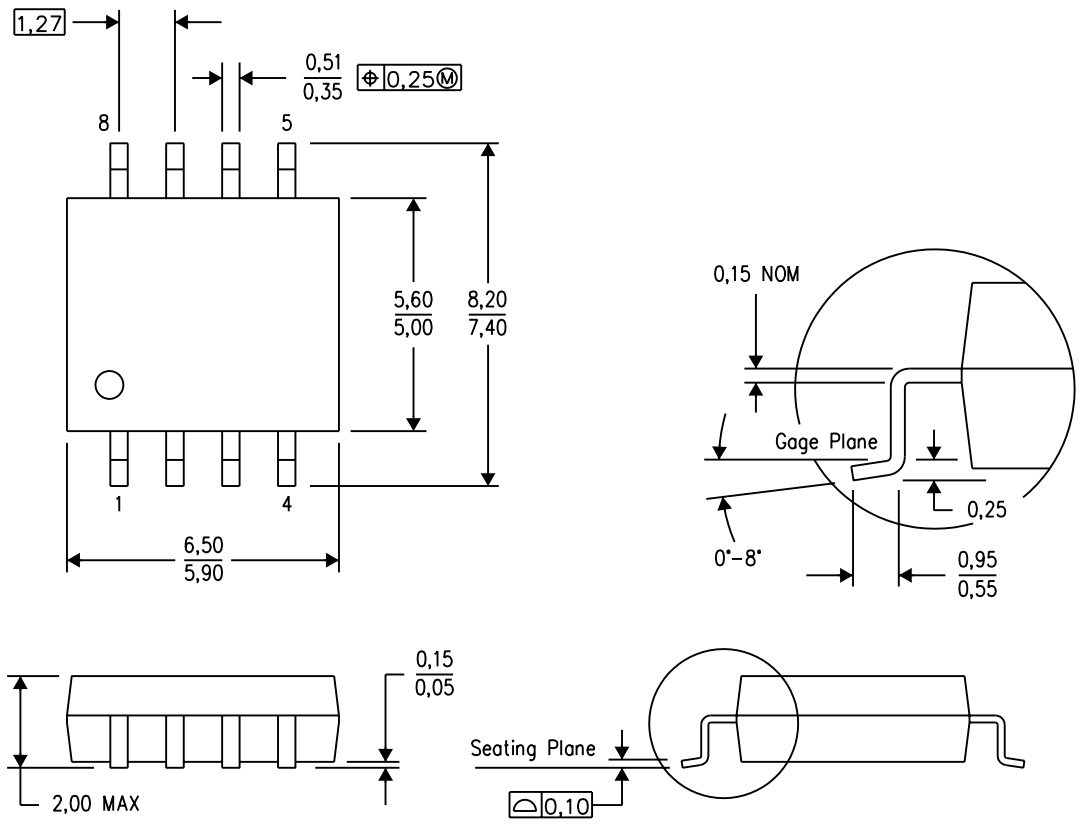
D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

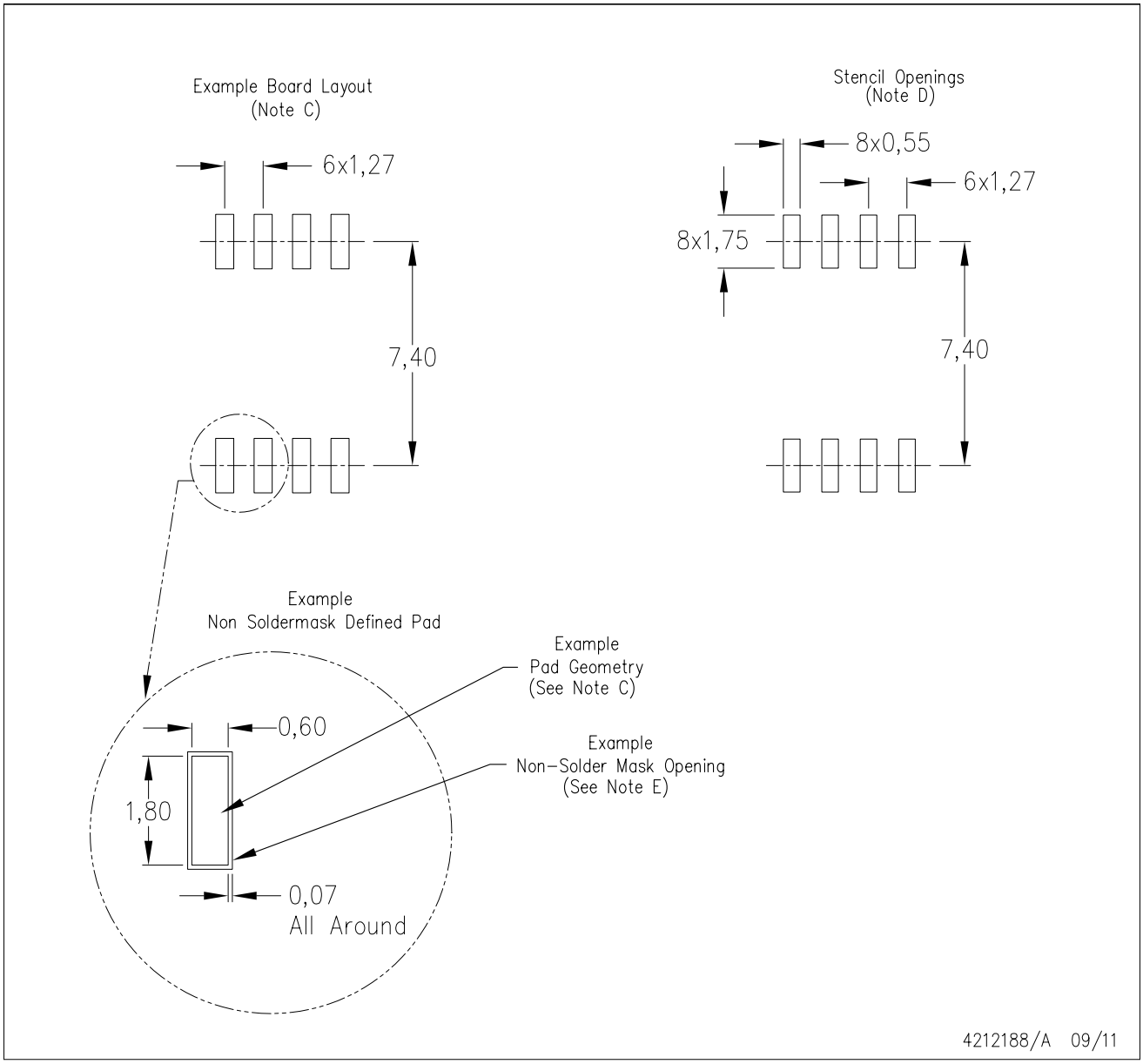
PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



4040063/C 03/03

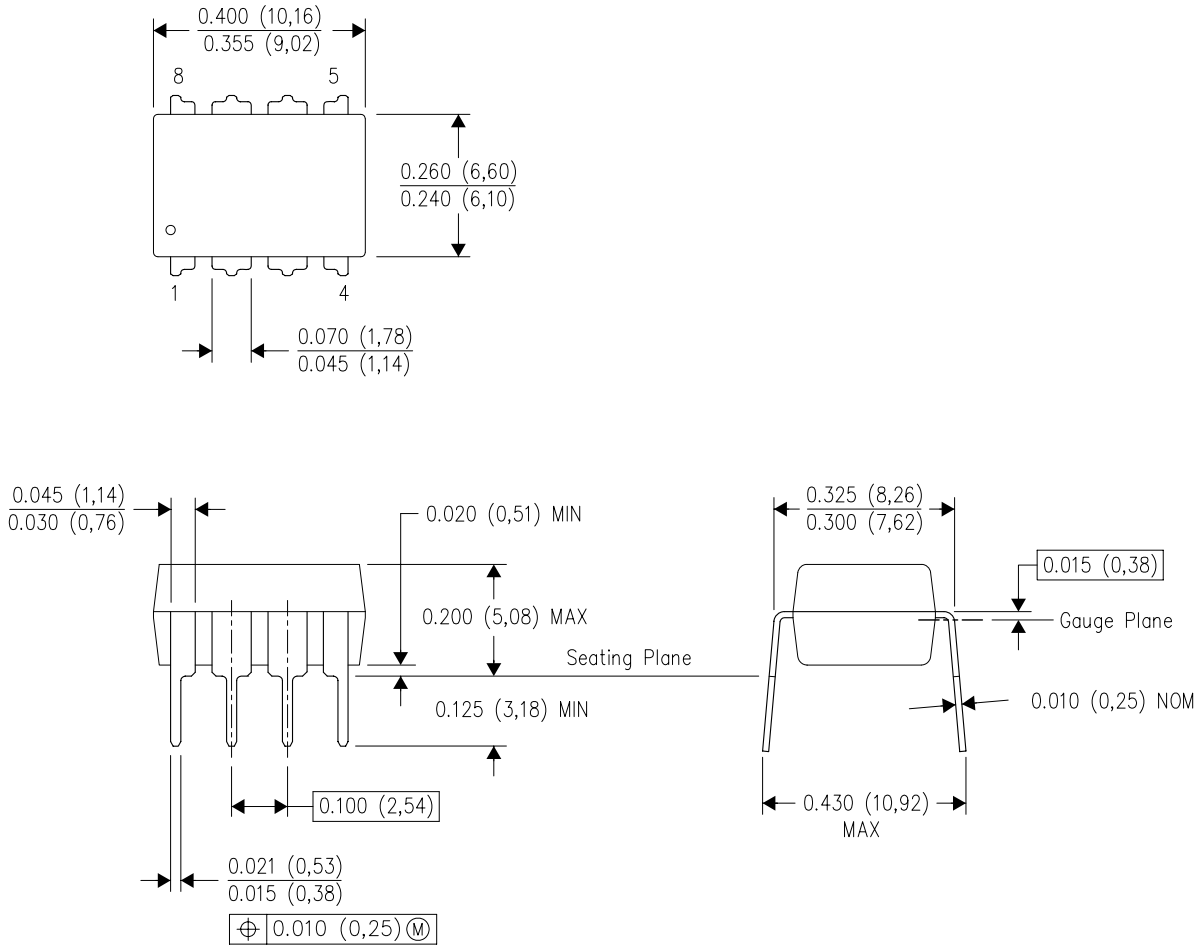
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.